Linearizer for a PIN Diode Attenuator

Tom L. Davis
2730 Timberleaf
Carrollton, TX 75006
Citizenship: United States of America

Kim E. Beumer
3404 Waltham Dr.
Richardson, TX 75082
Citizenship: Netherlands

Carey Ritchey
1613 Duke Court
Plano, TX 75093
Citizenship: Canada

RELATED APPLICATIONS

The present application is related to concurrently filed commonly assigned United States patent application serial number [49581-P030US-10104106] entitled "Broadband PIN Diode Attenuator Bias Network," the disclosure of which is hereby incorporated herein by reference.

TECHNICAL FIELD

The invention relates generally to attenuator circuitry and, more particularly, to circuitry to provide attenuation control linearly with respect to an attenuation control signal.

BACKGROUND

A common requirement in radio frequency (RF) circuits is the control of RF signal levels. For example, often in RF systems, such as CATV cable television systems, RF signal levels vary significantly resulting in unpredictable and/or undesired operation of particular components thereof, such as receivers, tuners, repeaters, and the like. Accordingly, such systems often utilize controllable signal attenuators, such as at the input stage of one of the aforementioned components, in order to provide a relatively constant RF signal level as provided to such components.

Often the above mentioned controllable attenuators are provided with a voltage controlled RF attenuator such as a linear attenuator. A linear attenuator typically has three ports or interfaces; those being an RF input port, an RF output port, and a control input. Ideally, a linear attenuator provides attenuation (generally expressed in decibels) between the RF input and RF output ports that is a linear function of a control input. Other desirable attributes of a linear attenuator include maintaining a good impedance match at the RF ports with respect the circuit coupled thereto over the control and frequency range, providing a flat attenuation response over a wide band of frequencies, introducing little or no excess noise into the circuit, and generating little or no distortion in the signals attenuated thereby. In RF systems that operate with signals of more than one octave of RF spectrum (broadband) the attenuator must also ensure that, in addition to acting as an attenuator, the RF impedance (return loss) of both the input and output of the attenuator is held as close as possible to the desired system impedance. Failure to maintain a proper impedance match can greatly affect the system frequency response (power transfer) and noise figure.

However, prior art linear attenuators generally provide a tradeoff with respect to these desirable attributes and, therefore, often provide less than ideal operation in demanding system applications. For example, there is generally a trade off between providing a flat attenuation response across a broadband signal and maintaining a good impedance match throughout the control and frequency range. Similarly, previous attenuation circuit

implementations have experienced a trade off between providing attenuation that is a linear function of the control input and providing a low insertion loss. Specifically, PIN diode attenuator circuits are available that will provide decibel per volt linearization, but typically will have a minimum of approximately 3 to 4 dB insertion loss.

One common implementation of a linear attenuator consists of a two section embodiment including a PIN diode attenuator section and a linearizer section coupled to the PIN diode attenuator section. In such a configuration, a PIN diode network, such as a π network or a T network, and passive bias components form the PIN diode attenuator section and provide attenuation of signals passed therethrough in response to a control voltage applied to the attenuator section. Specifically, the PIN diodes exhibit a variable RF resistance that is inversely proportion to the DC current through the diode and, therefore, the arrangement of PIN diodes and the corresponding bias components provides a circuit in which variable attenuation is achieved in response to a control voltage applied to bias components.

Such a PIN diode attenuator transfer function of RF attenuation versus DC current is non-linear due to the non-linear RF resistance of the PIN diodes versus bias current. Accordingly, a linearizer section is provided to allow a linear control voltage applied to an input of the linearizer section to result in a corresponding linear attenuation response of an RF signal applied to the PIN diode attenuator section.

Next-generation digital cable set-top boxes, such as those conforming to the OPENCABLE tuner specifications from Cable Television Laboratories, Inc., must provide attenuation in a large dynamic range (gain control range), such as on the order of 30 dB of dynamic range and beyond, while maintaining the RF input impedance of the device, such as 75 ohms. However, PIN diode attenuator configurations, such as those described above, have heretofore been unable to adequately address such requirements. For example, previously known T attenuator structures are precluded for use in the above conditions as 30 dB of dynamic range is not available with commercially available PIN diodes in the prior art T

network configurations. Similarly, previously known π attenuator structures, although perhaps able to achieve a relatively large dynamic range, generally are not able to maintain the return loss or impedance match over this dynamic range. For example, typical prior art π attenuator structures result in poor return loss in designs with more than 15 dB of attenuation.

Moreover, the linearizer section of such prior art linear attenuators are not adapted to maximize the performance of the pin diode structures based on minimum insertion loss of the device and the linearity, or the decibel insertion loss per volt structure of the gain control, while maintaining an optimized impedance match for the return loss of the attenuator over its entire attenuation range. Specifically, prior art linearizer sections generally do not provide decibel per volt linear gain control functions in a linear attenuator having a minimum insertion loss and which maintains the return loss of the attenuator over a range of attenuation greater than 15 dB. For example, there are prior art linear attenuators available that will provide a decibel per volt linearization, but typically will result in the attenuator operating at 3 or 4 dB of minimum insertion loss. Additionally, there are prior art linear attenuators available which attempt to act as a linearizer, however these linear attenuators have been unable to achieve a return loss of better than approximately 10 dB over a relatively wide dynamic operating range, such as 30 dB of dynamic attenuation. Such insertion losses and return loss levels are unacceptable in demanding system applications, such as systems conforming to next generation specifications for cable television equipment.

One prior art solution attempting to meet the above goals is to use a circuit that has break points, e.g., a portion of the desired dynamic range is provided within a first circuit break point and another portion of the desired dynamic range is provided within a second circuit break point. However, this solution suffers from the disadvantage that the attenuator must generally be manually adjusted for the break points. Moreover, the break points typically cause discontinuities in the transfer curve.

Accordingly, a need exists in the art for a linearizer circuit which operates a corresponding attenuator circuit relatively linearly with respect to an attenuation control

signal, such as decibel per volt linearization, while ensuring that the attenuator circuit maintains a desired return loss over a relatively large dynamic range, such as on the order of 30 dB.

SUMMARY OF THE INVENTION

The present invention is directed to a system and method in which a simple linearizer circuit is provided which approximates the ideal linearizer for PIN diode networks which are configured to provide controllable attenuators having a relatively low insertion loss over a relatively large dynamic range. Linearizers of the present invention are provided for various PIN diode network topologies, including a π network and a T network.

It should be appreciated that, given a perfect linearizer, a PIN diode attenuator, having the PIN diodes arranged in an appropriate topology and having a bias components coupled thereto, can approach the ideal. Unfortunately, a perfect linearizer must provide control currents to the PIN diodes that are highly non-linear and vary over several orders of magnitude. Current linearizer designs are complex and usually deviate significantly from the ideal.

Preferred embodiments of the present invention provide a linearizer which controls PIN diode attenuators by the application of control (bias) current at two control ports of the PIN diode network. Although one of the difficulties in meeting the goals of maintaining good return loss and a very linear attenuation is that the currents that are required to control the PIN diodes have to be very non-linear, in developing the present invention it was recognized that the non-linear transfer characteristics that the linearizer is to generate are very close to matching the equations of a bipolar transistor differential pair. Accordingly, the preferred embodiment linearizer circuit utilizes bipolar differential pair circuit portions in providing linear control of an attenuator circuit.

The foregoing has outlined rather broadly the features and technical advantages of the present invention in order that the detailed description of the invention that follows may be better understood. Additional features and advantages of the invention will be described hereinafter which form the subject of the claims of the invention. It should be appreciated by those skilled in the art that the conception and specific embodiment disclosed may be readily

utilized as a basis for modifying or designing other structures for carrying out the same purposes of the present invention. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the invention as set forth in the appended claims. The novel features which are believed to be characteristic of the invention, both as to its organization and method of operation, together with further objects and advantages will be better understood from the following description when considered in connection with the accompanying figures. It is to be expressly understood, however, that each of the figures is provided for the purpose of illustration and description only and is not intended as a definition of the limits of the present invention.

BRIEF DESCRIPTION OF THE DRAWING

For a more complete understanding of the present invention, reference is now made to the following descriptions taken in conjunction with the accompanying drawing, in which:

FIGURES 1A and 1B show PIN diode attenuator configurations such as may be controlled by linearizer circuitry of the present invention;

FIGURE 2 shows a bipolar transistor differential pair as may be utilized according to a preferred embodiment in providing control current output; and

FIGURE 3 shows a preferred embodiment linearizer circuit of the present invention.

DETAILED DESCRIPTION

The linearizer of the preferred embodiment of the present invention is adapted to operate with an attenuator topology having two attenuator control inputs. Although the complexity of the linearizer circuitry is increased by the preferred embodiment multiple control current configuration, this configuration allows control of diode currents independently of each other and, therefore, attenuator circuits may be controlled for optimized insertion loss and return loss at any given point of their dynamic range. Moreover, the recognition in developing the present invention that non-linear behavior exhibited by PIN diodes approximates the characteristics of a differential pair, such as a bipolar junction transistor differential pair or a MOSFET differential pair operated in the sub-threshold region, has been leveraged according to the preferred embodiment in providing a simplified multiple control signal output linearizer circuit according to the present invention.

A PIN diode attenuator operable with linearizers of the present invention is provided by connecting PIN diodes in a π network wherein the cathodes of all PIN diodes in the π network are DC grounded, such as through large value inductors coupling the cathodes to DC ground, providing a common cathode point bias voltage which is constant. This attenuator topology provides for a control current to be applied to the π network shunt diodes and series diode(s) separately. A preferred embodiment of a PIN diode π network is shown in FIGURE 1A and is described in detail in the above referenced patent application entitled "Broadband PIN Diode Attenuator Bias Network." Specifically, FIGURE 1A presents a complete circuit for an attenuator that employs an unbalanced, symmetrical π network of PIN diodes. RF input port (RF_{in}) and RF output port (RF_{out}) accept an RF signal to be attenuated using PIN diodes D1-D4 and output an attenuated RF signal, respectively. Attenuation control signal port SP_1 and attenuation signal control port SP_2 receive bias currents from the linearizer (I_1 and I_2, respectively) to control the RF resistances of diodes D1-D4. Capacitors C1 and C2 are DC blocking capacitors and capacitors C3, C4, and C5 provide RF shorts to ground. Inductors L1, L2, and L3 pass bias currents but present a high impedance at RF frequencies.

Resistors R1 and R2 serve to decouple the anodes of diodes D1 and D4 and, thus, provide blocking of a possible RF leakage path.

Another embodiment of a PIN diode attenuator operable with linearizers of the present invention is provided by connecting the PIN diodes in a T network wherein the cathodes of all PIN diodes in the T network are DC grounded, such as through a large value inductor coupling the cathodes to DC ground, providing a common cathode point bias voltage which is constant. As with the preferred embodiment π network discussed above, the preferred embodiment T network arrangement provides for control current to be applied to the T network shunt diode and series diodes separately. A preferred embodiment of a PIN diode T network, having an RF input port, an RF output port, attenuation control signal port SP_1, and attenuation control signal port SP_2, is shown in FIGURE 1B and is described in detail in the above referenced patent application entitled "Broadband PIN Diode Attenuator Bias Network."

In developing a linearizer circuit according to the present invention for use with a PIN diode attenuator, such as those employing topologies as discussed above with respect to preferred embodiment PIN diode attenuators, it was necessary to determine how to generate proper input control currents for the attenuator to achieve a desired or commanded level of attenuation (A) while maintaining the RF input impedance of the device throughout the dynamic range of attenuation.

Initially it is noted that PIN diode RF resistance (R) is a function of the DC current (I) flowing through the diode. An accepted mathematical model of this operation of a PIN diode is represented below.

$$R = \frac{K}{I^a} + R_s \qquad (1)$$

In the above equation, K, α, and R_S are constants which vary with diode type and packaging. Experimentation has revealed, however, that the series resistance (R_S) is normally on the order of one ohm and that the exponent α is usually just less than 1, such as on the order of 0.8 or 0.9 for typical PIN diodes.

Preferred embodiments of the present invention provide for a relatively large dynamic attenuation range, such as on the order of 30 dB. Accordingly, it is desirable to represent the commanded level of attenuation A in decibels as a scaled function that is mathematically convenient. The following linear scalar of A provides a suitable mathematical scaling.

$$\theta = \frac{\ln(10)}{20} A \qquad (2)$$

Accordingly, θ is used herein as a scaled function of the commanded attenuation A (preferably in decibels) in solving for the appropriate control signals to be applied by a linearizer of the present invention to the control inputs of a PIN diode attenuator.

In developing a preferred embodiment linearizer, the following equations were used to represent the resistances PIN diodes disposed in a π attenuator circuit should ideally obey.

$$R_A = \frac{Z_0}{2} \sinh(\theta) \qquad (3)$$

$$R_B = \frac{Z_0}{\tanh\left(\frac{\theta}{2}\right)} \qquad (4)$$

Specifically, R_A represents the RF resistance (in ohms) of diodes disposed in a series configuration, e.g., diodes D2 and D3 of FIGURE 1A. Similarly, R_B represents the RF resistance (in ohms) of diodes disposed in a shunt configuration, e.g., diodes D1 and D4 of FIGURE 1B. Z_0 is the characteristic impedance of the system, such as might be 75 ohms in a typical CATV application.

Substituting the series and shunt resistances, equations (3) and (4), into the PIN diode model equation, equation (1), and solving for the current (I) provides the following equations, respectively, wherein the subscripts 1 and 2 represent the series and shunt elements, and wherein the multiplier 2 is provided to accommodate providing the control current to 2 series or shunt diodes of the preferred embodiment.

$$I_1 = 2\left[\frac{2K_1}{Z_o \sinh(\theta) - 2R_{s1}}\right]^{\frac{1}{a_1}} \qquad (5)$$

$$I_2 = 2\left[\frac{K_2 \tanh\left(\frac{\theta}{2}\right)}{Z_o - R_{s2}\tanh\left(\frac{\theta}{2}\right)}\right]^{\frac{1}{a_2}} \qquad (6)$$

It should be appreciated that the above equations provide a mathematical representation of the circuit bias currents as a function of commanded attenuation for a PIN diode attenuator such as that shown in FIGURE 1A. Moreover, it should be appreciated that

the above equations provide the inverse mathematical representation of the circuit bias currents as a function of commanded attenuation for a PIN diode attenuator such as that shown in FIGURE 1B, e.g., $1 / I_1$ and $1 / I_2$, respectively. Accordingly, the above equations may be utilized in designing a linearizer circuit for use with PIN diode attenuators.

However, it is readily apparent that the above circuit bias equations, equations (5) and (6), do not easily lend themselves to a circuit implementation. Specifically, these two equations are very complex and a straight forward, non-linear circuit implementation of these equations would be extremely complex and would likely suffer stability problems. Accordingly, in developing the preferred embodiment linearizer the above equations were simplified for circuit implementation.

Experimentation and simulation has shown that the circuit bias equations, equations (5) and (6), may be simplified in a number of ways. For example, as mentioned above, the constant α for typical PIN diodes has been found to be generally on the order of 0.8 or 0.9 and, therefore, the exponents $1/\alpha_1$ and $1/\alpha_2$ may be approximated as 1. The series resistance R_S is of a low enough value that its being dropped from the equations for purposes of simplification should still provide a suitable approximation.

Using the approximations discussed above, as well as assumptions as discussed below, the circuit bias equations, equations (5) and (6), were simplified as shown below.

$$I_1 = \frac{8K_1}{Z_o\left(\exp(\theta) - 1\right)} \qquad (7)$$

$$I_2 = \frac{2K_2}{Z_o - R_{s2}} \tanh\left(\frac{\theta}{2}\right) \qquad (8)$$

In simplifying circuit bias equation (5) to arrive at simplified circuit bias equation (7), it was appreciated that $\sinh(\theta) = (e^{\theta} - e^{-\theta})/2$. Making the assumption that $e^{-\theta}$ may be approximated as 1, $\sinh(\theta)$ was replaced by $(e^{\theta} - 1)/2$ in circuit bias equation (7). Similarly, in simplifying circuit bias equation (6) to arrive at simplified circuit bias equation (8), it was assumed that the hyperbolic tangent in the denominator could be assumed to be approximately one and, therefore, dropped from the circuit bias equation.

Having arrived at a simplified representation of the circuit bias currents to be provided to the diode attenuator for linearized operation, the simplified circuit bias equations, equations (7) and (8), were transformed into a non-linear circuit implementation. Specifically, in providing the preferred embodiment linearizer circuit implementation, the simplified circuit bias equations were related to a transistor differential pair, such as the differential pair of FIGURE 2. The differential pair of FIGURE 2 includes transistors Q_a and Q_b coupled in a circuit such that $I_a = e^{((Va - Ve) / Vt)}$ and $I_b = e^{((Vb - Ve) / Vt)}$, where V_t is the thermal voltage.

The approximation for the series control signal (I_1) can be realized as the collector current I_b using the differential pair of FIGURE 2 by setting $V = V_t \theta$ and driving the emitter current, I_{EE}, so that the collector currents have the constant offset $I_a - I_b = (8 K_1) / Z_0$. The approximation for the shunt control signal (I_2) can be realized as the difference between the collector currents $I_b - I_a$ using the differential pair of FIGURE 2 by setting $V = V_t \theta$ and the emitter current $I_{EE} = (2 K_2) / (Z_0 - R_{S2})$. Accordingly, it should be appreciated that PIN diodes which are well modeled by equation (1) above, $0.7 \leq \alpha \leq 1$, $Z_0 >> R_s$, are well suited for use in a diode attenuator for which control is provided by a linearizer of the present invention.

Directing attention to FIGURE 3, a preferred embodiment linearizer circuit utilizing differential pairs to provide a series control signal (I_1) and a shunt control signal (I_2) as described above is shown as linearizer circuit 300. Specifically, differential pair 301, including transistors Q1 and Q2, is utilized in linearizer circuit 300 in providing series control

signal I_1 and differential pair 302, including transistors Q3 and Q4, is utilized in linearizer circuit 300 in providing shunt control signal I_2.

As discussed above, according to the preferred embodiment the base voltage for the transistors disposed in the differential pair is preferably set to $V_t \theta$. However, this control voltage has a temperature dependency because of the presence of V_t in the equation, where $V_t = k T / q$, where k is Boltzmann's constant and q is the charge of an electron. Accordingly, without compensating circuitry, changes in temperature would result in changes in the control currents provided by linearizer circuit 300. In order to compensate for this temperature behavior, the control voltage of the preferred embodiment is multiplied by a PTAT (Proportional To Absolute Temperature) quantity. For example, compensation for the temperature variant V_t may be done by multiplying the control voltage input and the PTAT voltage (V1) in linear multiplier (M1). The resulting temperature compensated control voltage may then be used to drive the two differential pairs as described above.

It should be appreciated that although a base voltage differential across the transistors of the differential pairs is illustrated as being with respect to a ground (the base of transistors Q2 and Q3 illustrated as being at a ground potential), it should be appreciated that the voltage $V_t \theta$, may be provided as a differential voltage. For example, the ground coupled to the bases of transistors Q2 and Q3 may be a DC ground having a potential (whether positive or negative) with respect to zero potential ground. Accordingly, $V_t \theta$ may be provided as a differential potential.

In providing series control signal I_1, the preferred embodiment linearizer circuit shown in FIGURE 3 synthesizes the simplified series circuit bias equation, equation (7), using transistors Q1, Q2, Q5, Q6, and Q7. Transistors Q1 and Q2 provide differential pair 301 while transistors Q5, Q6, and Q7 provide current mirror 311 used in providing series control current I_1 equal to the collector current of Q2. Gain block (G1) forces the difference of the collector current of Q1 and Q2 to be equal to the current I_{s1} by controlling the tail

current (I_{EE}) of differential pair Q1 and Q2. The collector current of transistor Q2 , which is the current I_1 as given by equation (5), is mirrored for output by transistor Q7.

It should be appreciated that current I_{s1}, $(8\ K_1) / Z_0$ in the preferred embodiment, is dependent upon the characteristics of the particular PIN diodes utilized in implementing the attenuator controlled using linearizer circuit 300. Specifically, as discussed above with respect to the mathematical model of operation of PIN diodes, equation (1), the constant K_1 varies with diode type and packaging. Accordingly, a preferred embodiment of current source 321 providing current I_{s1} is programmable, such as by digital input or use of a control circuit, to accommodate the use of PIN diodes having different characteristics associated therewith. Similarly, preferred embodiment current sources of the present invention may include programmable or adjustable current adjustment to compensate for thermal variations of the PIN diode structures, such as by providing properly compensated control currents in response to monitored operational temperature.

In providing shunt control signal I_2, the preferred embodiment linearizer circuit shown in FIGURE 3 synthesizes the simplified shunt circuit bias equation, equation (8), using transistors Q3, Q4, Q8, and Q9. Transistors Q3 and Q4 provide differential pair 302 while transistors Q8 and Q9 provide current mirror 312 used in providing shunt control current I_2 equal to the difference between the collector current of Q4 and the collector current of Q3. Tail current I_{EE} is set to the desired value as discussed above. The current mirror provided by transistors Q8 and Q9 subtracts the collector current of Q3 from Q4 to thereby provide the desired output shunt control current I_2.

It should be appreciated that current I_{EE}, $(2\ K_2) / (Z_0 - R_{S2})$ in the preferred embodiment, is dependent upon the characteristics of the particular PIN diodes utilized in implementing the attenuator controlled using linearizer circuit 300. Specifically, as discussed above with respect to the mathematical model of operation of PIN diodes, equation (1), the constants K_2 and R_{S2} vary with diode type and packaging. Accordingly, a preferred embodiment of current source 322 providing current I_{EE} is programmable, such as by digital

input or use of a control circuit, to accommodate the use of PIN diodes having different characteristics associated therewith. Similarly, preferred embodiment current sources of the present invention may include programmable current adjustment to compensate for thermal variations of the PIN diode structures, such as by providing properly compensated control currents in response to monitored operational temperature.

Having described a preferred embodiment linearizer circuit of the present invention in detail, it should be appreciated that various alterations may be made thereto in accordance with the principals of the present invention as disclosed herein. For example, in order to provide a linearizer circuit with relatively low power requirements, alternative embodiments of the present invention may utilize current multipliers between the linearizer circuit implementation and the control current outputs of the present invention. Accordingly, an alternative embodiment of linearizer circuit 300 includes a linear multiplication factor in current mirror 311 or after current mirror 312 to thereby provide a desired control current level which is greater than the operating currents of the differential pairs. Similarly, although the preferred embodiment linearizer circuit 300 has been discussed above with reference to a π network PIN diode attenuator, it should be appreciated that the disclosed linearizer circuit may be utilized with other attenuator configurations. For example, linearizer circuit 300 may be utilized in controlling a T network PIN diode attenuator by using appropriate circuits to compute the reciprocal of each of the output currents I_1 and I_2.

Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure of the present invention, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to

be developed that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the present invention. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.